IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended: A semiconductor device, comprising:

a first transistor including a first source region, a first drain region provided in ~~the~~ a same device region as the first source region, and a first ~~loop-shaped~~ gate electrode region; and

a second transistor including ~~sharing, with the first transistor, the loop-shaped~~ a second gate electrode region electrically coupled with the first gate electrode region of the first transistor, ~~and the~~ a second source region, and ~~or the~~ a second drain region provided in a same device region as the second source region,

wherein the first and the second gate electrode regions form a loop-shaped gate electrode region arranged to surround a part of the device region and at least one device isolation region.

Claim 2 (Currently Amended): A semiconductor device, comprising:

a device region where each of a plurality of source regions and each of a plurality of drain regions of transistors are alternately included; and

a plurality of loop-shaped gate electrode regions of the transistors which are formed on the device region, ~~and part of which are~~ each of the loop-shaped gate electrode being disposed onto two positions between the source regions and the drain regions, the loop-shaped electrode region is arranged to surround a part of the device region and at least one device isolation region.

Claim 3 (Withdrawn-Currently Amended): A semiconductor device, comprising:

a first device region including a plurality of source regions and a plurality of drain regions of first conductivity type transistors;

a plurality of loop-shaped gate electrode regions of the first conductivity type transistors, each of the gate electrode regions ~~being~~ formed on the first device region;

a second device region including a plurality of source regions and a plurality of drain regions of a second conductivity type transistors;

a plurality of loop-shaped gate electrode regions of the second conductivity type transistors, each of the gate electrode regions ~~being~~ formed on the second device region and electrically coupled to each of the gate electrode regions of the first conductivity type transistors;

a first wiring configured to supply a first voltage to at least one of the source regions of the first device region;

a second wiring configured to supply a second voltage to at least one of the source regions of the second device region; and

a third wiring electrically coupled to the drain regions of the first and second device regions and to the gate electrode regions of the first and the second conductivity type transistors.

Claim 4 (Original): The semiconductor device of claim 1, wherein the drain region is formed in a region surrounded by the loop-shaped gate electrode region.

Claim 5 (Currently Amended): The semiconductor device of claim 1, wherein ~~an~~ a plurality of electrically independent drain regions is formed in a region surrounded by the loop-shaped electrode region.

Claim 6 (Original): The semiconductor device of claim 1, wherein the source region is formed outside a region surrounded by the loop-shaped gate electrode region.

Claim 7 (Original): The semiconductor device of claim 1, wherein a plurality of the source regions are formed outside a region surrounded by the loop-shaped gate electrode region, the plurality of the source regions electrically coupled to each other.

Claim 8 (Currently Amended): The semiconductor device of claim 1, wherein ~~the~~ respective loop-shaped gate electrode regions have same lengths on the device region and ~~a~~ the device isolation region except contact regions between wiring portions and the gate electrode regions.

Claims 9-10 (Canceled).

Claim 11 (Currently Amended): The semiconductor device of claim ~~10~~ 3, wherein the gate electrode regions of the first and the second conductivity type transistors are coupled by a wiring.

Claim 12 (Currently Amended): The semiconductor device of claim ~~10~~ 3, wherein the gate electrode regions of the first and second conductivity type transistors are coupled by a region made of a material to form the gate electrode regions.

Claim 13 (Withdrawn): The semiconductor device of claim 3, wherein a shape of the gate electrode region of the first conductivity type transistor is different from that of the gate electrode region of the second conductivity type transistor.

Claim 14 (Withdrawn): The semiconductor device of claim 3, wherein a shape of the first device region is different from that of the second device region.

Claim 15 (Withdrawn): The semiconductor device of claim 3, wherein a channel region of the first or the second conductivity type transistor is formed in a plane perpendicular to a substrate surface.

Claim 16 (Withdrawn): The semiconductor device of claim 15, wherein a direction of an electric current flowing through the channel region of the first or second conductivity type transistor is horizontal to the substrate surface.

Claim 17 (Withdrawn): The semiconductor device of claim 3, wherein the first or the second device region includes a fin structure including a plurality of rectangular strips.

Claim 18 (Withdrawn): The semiconductor device of claim 17, wherein, in the semiconductor device, a plurality of channel regions are formed in perpendicular to a substrate surface, a direction of an electric current is horizontal to the substrate surface, and the channel regions are completely depleted during operation.

Claim 19 (Withdrawn): The semiconductor device of claim 18, wherein a ratio of a number of fins of the channel of an n-type transistor to a number of fins of the channel of a p-type transistor of the semiconductor device is 1.0 or more and 2.0 or less.

Claim 20 (Withdrawn): A manufacturing method of a semiconductor device, comprising:

depositing a hard mask material on a gate electrode material;

forming a dummy gate pattern on the deposited hard mask material;

depositing a material for forming a sidewall around the dummy gate pattern;

etching the material for forming the sidewall while the sidewall is left;

selectively removing the dummy gate pattern;

depositing resist, by lithography, to form a region coupling a gate electrode with a metal wiring;

processing a hard mask of a gate electrode region;

removing the resist; and

processing the gate electrode region using the hard mask.

Claim 21 (New): The semiconductor device of claim 1, wherein the device isolation region is arranged aside the device region perpendicular to a direction of current flowing from the first source region to the first drain region in the first transistor.

Claim 22 (New): The semiconductor device of claim 1, wherein the loop-shaped electrode region is arranged to surround two device isolation regions, and said two device

isolation regions are arranged at both sides of the device region perpendicular to a direction of current flowing from the first source region to the first drain region in the first transistor.